FORM PTO-1390 (REV 10-2000) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 42390.P6624PCT

U.S. APPLICATION NO (If known, see 37 CFR 1 5): 09/831539

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US99/26224 ✓	November 5, 1999 ✓	November 12, 1998 ✓

TITLE OF INVENTION: FIELD EFFECT TRANSISTOR STRUCTURE WITH ABRUPT SOURCE/DRAIN JUNCTIONS

APPLICANT(S) FOR DO/EO/US: MURTHY ET AL. Anand.S

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U S C. 371
3. [ ] This is an express request to promptly begin national examination procedures (35 U S C. 371(f))
4. [X] The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [X] is attached hereto (required only if not communicated by the International Bureau).
   b. [ ] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Of fice (RO/US).
6. [ ] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. [X] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [X] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English language translation of the annexes to the International Preliminary Examination Repo rt under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [ ] A change of power of attorney and/or address letter.
16. [X] Other items or information:

    Request for Priority

09/831539 (see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO PCT/US99/26224	ATTORNEY'S DOCKET NUMBER 42390.P6624PCT

17. [X] The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

	CALCULATIONS PTO USE ONLY
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $860.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) $690.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 1000.00
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	30 - 20 =	10	X $18.00	$ 180.00
Independent claims	4 - 3 =	1	X $80.00	$ 18.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$
TOTAL OF ABOVE CALCULATIONS =				$ 1258.00
[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$
SUBTOTAL =				$ 1258.00
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$
TOTAL NATIONAL FEE =				$ 1258.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$
TOTAL FEES ENCLOSED =				$ 1258.00
			Amount to be refunded:	$
			charged:	$

a. [X] A check in the amount of $ 1258.00 to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-2666. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO

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FIELD EFFECT TRANSISTOR STRUCTURE WITH ABRUPT SOURCE/DRAIN JUNCTIONS

Background of the Invention

Field of the Invention

The invention relates to metal-oxide-semiconductor field effect transistors (MOSFETs) and more particularly to transistor structures having abrupt junctions, and methods of making same.

Background

The trend of integrating more functions on a single substrate while operating at ever higher frequencies has existed in the semiconductor industry for many years. Advances in both semiconductor process technology and digital system architecture have aided in producing these more highly integrated and faster operating integrated circuits.

The desired result of many recent advances in semiconductor process technology has been to reduce the dimensions of the transistors used to form the individual circuits found on integrated circuits. There are several well-recognized benefits of reducing the size of transistors. In the case of MOSFETs, reducing the channel length provides the capability to deliver a given amount of drive current with a smaller channel width. By reducing the width and length of a FET, the parasitic gate capacitance, which is a function of the area defined by the width and length can be reduced, thereby improving circuit performance. Similarly, reducing the size of transistors is beneficial in that less area is consumed for a given circuit, and this allows more circuits in a given area, or a smaller, less costly chip, or both.

It has also been well known that MOSFETs can not simply be scaled down linearly. That is, as the width and length attributes of a MOSFET are reduced, other parts of the transistor, such as the gate dielectric and the junctions must also be scaled so as to achieve the desired electrical characteristics. Undesirable electrical characteristics in MOSFETs due to improper scaling include coupling of the electric field into the channel region and increased subthreshold conduction. These effects are sometimes referred to in this field as short channel effects.

A number of methods have been developed to form ever more shallow source/drain junctions for MOSFETs in order to achieve proper scaling. Unfortunately, these very shallow junctions create source/drain extensions that have increased resistivity as compared with deeper source/drain junctions. In longer channel length MOSFETs with deeper source/drain junctions, the source/drain extension resistivity was negligible compared to the on-resistance of the MOSFET itself. However, as MOSFET channel lengths decrease into the deep sub-micron region, the increased source/drain extension resistivity becomes a significant performance limitation.

What is needed is a field effect transistor structure having very short channel length and low source/drain extension resistivity, yet operable to produce high drive currents without suffering from the short channel effects that produce significant levels of off-state current. What is further needed is a method of manufacturing such a structure.

Summary of the Invention

Briefly, a MOSFET structure includes highly conductive source/drain extensions of a first conductivity type, and super abrupt junctions with a semiconductor body of a second conductivity type.

In a further aspect of the invention, a process for forming a MOSFET includes removing portions of the substrate to form recesses that are adjacent and partially subjacent a FET gate structure, and back filling the recesses with an epitaxial process.

Brief Description of the Drawings

Fig. 1 is a schematic cross-section of a wafer in process showing a substrate with a gate dielectric formed thereon, and a patterned gate electrode over the gate dielectric and a spacer layer formed over the surface of the wafer.

Fig. 2 is a schematic cross-section showing the structure of Fig. 1, after an anisotropic etch of the spacer layer forms thin sidewall spacers, and the gate dielectric not covered by the gate electrode or sidewall spacers is removed.

Fig. 3 is a schematic cross-section showing the structure of Fig. 2, after an isotropic etch removes portions of the substrate, to form recesses therein, and further showing a portion of the gate electrode etched away.

Fig. 4 is a schematic cross-section showing the structure of Fig. 3, after the recesses have been back-filled and the gate electrode thickness built up.

Fig. 5 is a schematic cross-section showing the structure of Fig. 4, after a salicidation operation.

Fig. 6 is a schematic cross-section showing the structure of Fig. 3, after an alternative process flow in which the back-filling of the recesses includes forming a layer of a first conductivity type followed by formation of a layer of a second conductivity type.

Fig. 7 is a flow diagram illustrating the various operations in a manufacturing process in accordance with the present invention.

Detailed Description

Overview

Conventional source/drain junction formation is accomplished by an ion implantation operation that is self-aligned to the gate electrode, or alternatively, aligned to sidewall spacers that are adjacent to the gate electrode. Reasonable transistor performance has been achieved in this way for many generations of semiconductor process technology. However, as transistor scaling has brought FET channel lengths down into the deep sub-micron region, the changes to source/drain junction depth and doping concentration required to achieve desirable electrical performance of FETs have increased the parasitic resistance associated with the FET source/drain terminals to the point where this parasitic resistance is significant compared to the on-resistance of the FET. In this field, the parasitic resistance is sometimes referred to as external resistance. More particularly, simultaneously obtaining the very shallow junction depth, high source-drain extension doping concentration, and abrupt change in doping profile between the body and source/drain junctions, all required for desirable electrical performance in deep submicron FETs has become extremely difficult to achieve with conventional processes.

An illustrative embodiment of the present invention provides a FET with highly conductive source/drain extensions and abrupt junctions. Methods of forming the FET structure of the present invention include isotropically etching the substrate adjacent to, and partially underneath, the gate dielectric layer of a FET, and selectively depositing bilayers of in-situ doped material of a first conductivity type, and a second conductivity type.

FETs embodying the present invention include back-filled source and drain terminals. In this way, the doping concentration of the source/drain terminals can be controlled by controlling the gas mixture, temperature, and pressure, in a reaction chamber. With the precise control of doping concentration of the material being deposited, the embodiments of the present invention include microelectronic devices having very abrupt junctions. Furthermore, particular embodiments of the present invention may eliminate high-energy ion implantation of the source/drain junctions. Formation of the source/drain junctions in this way also provides increased margin for the process thermal budget, since a high temperature operation is not required to activate the dopants, or to thermally in-diffuse the dopants into the tip portion of the source/drain terminals.

Terminology

The terms, chip, integrated circuit, monolithic device, semiconductor device, and microelectronic device, are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

The terms metal line, trace, wire, conductor, signal path and signaling medium are all related. The related terms listed above, are generally interchangeable, and appear in order from specific to general. In this field, metal lines are sometimes referred to as traces, wires, lines, interconnect or simply metal. Metal lines, generally aluminum (Al), copper (Cu) or an alloy of Al and Cu, are conductors that provide signal paths for coupling or interconnecting, electrical circuitry. Conductors other than metal are available in microelectronic devices. Materials such as doped polysilicon, doped single-crystal silicon (often referred to simply as diffusion,

regardless of whether such doping is achieved by thermal diffusion or ion implantation), titanium (Ti), molybdenum (Mo), cobalt (Co), nickel (Ni) and tungsten (W) and refractory metal silicides are examples of other conductors.

The terms contact and via, both refer to structures for electrical connection of conductors from different interconnect levels. These terms are sometimes used in the art to describe both an opening in an insulator in which the structure will be completed, and the completed structure itself. For purposes of this disclosure contact and via refer to the completed structure.

Epitaxial layer refers to a layer of single crystal semiconductor material.

The term "gate" is context sensitive and can be used in two ways when describing integrated circuits. As used herein, gate refers to the insulated gate terminal of a three terminal FET when used in the context of transistor circuit configuration, and refers to a circuit for realizing an arbitrary logical function when used in the context of a logic gate. A FET can be viewed as a four terminal device when the semiconductor body is considered.

Polycrystalline silicon is a nonporous form of silicon made up of randomly oriented crystallites or domains. Polycrystalline silicon is often formed by chemical vapor deposition from a silicon source gas or other methods and has a structure that contains large-angle grain boundaries, twin boundaries, or both. Polycrystalline silicon is often referred to in this field as polysilicon, or sometimes more simply as poly.

Source/drain terminals refer to the terminals of a FET, between which conduction occurs under the influence of an electric field, subsequent to the inversion of the semiconductor surface under the influence of an electric field resulting from a voltage applied to the gate terminal. Source/drain terminals are typically formed in a semiconductor substrate and have a conductivity type (i.e., p-type or n-type) that is the opposite of the conductivity type of the substrate. Sometimes, source/drain terminals are referred to as junctions. Generally, the source and drain terminals are fabricated such that they are geometrically symmetrical. Source/drain terminals may include extensions, sometimes referred to as tips, which are shallower than other portions of the source/drain terminals. The tips typically extend toward the channel region of a FET, from

the main portion of the source/drain terminal. With geometrically symmetrical source and drain terminals it is common to simply refer to these terminals as source/drain terminals, and this nomenclature is used herein. Designers often designate a particular source/drain terminal to be a "source" or a "drain" on the basis of the voltage to be applied to that terminal when the FET is operated in a circuit.

Substrate, as used herein, refers to the physical object that is the basic workpiece that is transformed by various process operations into the desired microelectronic configuration. A substrate may also be referred to as a wafer. Wafers, may be made of semiconducting, non-semiconducting, or combinations of semiconducting and non-semiconducting materials.

The term vertical, as used herein, means substantially perpendicular to the surface of a substrate.

Referring to Figs. 1-6, an illustrative embodiment of the present invention is described. As shown in Fig. 1, a wafer is processed in known ways to form a thin film layer over a patterned gate electrode and over a gate dielectric layer that has been disposed on the top surface of the wafer. More particularly, as shown in Fig. 1, a substrate **102** has a gate dielectric layer **104** disposed over the surface thereof, and a patterned gate electrode **106** is formed over gate dielectric layer **104**. In the illustrative embodiment, substrate **102** is a silicon wafer, gate dielectric layer **104** is a silicon dioxide layer, and gate electrode **106** is formed from polysilicon. Although gate dielectric layer **104** is typically a thin layer of oxidized silicon, the thickness and chemical make-up of the gate insulator layer may be varied within the scope of the invention.

Those skilled in the art and having the benefit of this disclosure will recognize that although field oxide regions are not shown in the Figures, the operations and structures shown and described herein, are compatible with various field oxide isolation architectures. Examples of field oxide isolation architectures include shallow trench isolation regions in a surface of a substrate, and the older local oxidation of silicon, which formed non-planarized oxide isolation regions.

A thin film layer **108** is deposited over the surface of gate electrode **106** and the portions of gate dielectric layer **104** not already covered by gate electrode **106**. Thin film layer **108** may also be referred to as a spacer layer because spacers adjacent to the side walls of gate electrode **106** are formed from layer **108** in subsequent processing operations. It is preferable for spacer layer **108** to have etch characteristics that are different from the etch characteristics of substrate **102** and gate electrode **106**. The material for spacer layer **108** could be any dielectric material including, but not limited to, nitride, oxynitride, and oxide. In the illustrative embodiment, subsequent to the polysilicon etch that forms gate electrode **106**, a thin layer of silicon nitride is deposited over the surface of the substrate to form spacer layer **108**. In one embodiment, the silicon nitride layer is approximately 20 nm thick, and is formed in a vertical diffusion furnace. However, the thickness of the nitride layer is not a limitation of the invention and it may be made any practical thickness, for example, in a range of from 2 nm to 50 nm thick. This nitride layer will be used to provide the needed selectivity during a subsequent epitaxial backfill operation. Similarly, the spacer layer may be formed of another material such as, for example, silicon dioxide. Silicon dioxide has a dielectric constant that is lower than the dielectric constant of silicon nitride, and this is advantageous in terms of lowering parasitic capacitance between the gate electrode and other nearby circuit nodes.

Referring to Fig. 2, spacer layer **108** is etched anisotropically using, for example, conventional dry etch chemistries for silicon nitride. Subsequent to this etch operation, no significant amount of residual silicon nitride remains in the source/drain regions. In the illustrative embodiment, this anisotropic etch operation leaves a nitride layer approximately 150nm thick (when measured along a vertical axis) along the sidewalls of polysilicon gate electrode **106**. Typically, the vertical height (i.e., thickness) of this layer is approximately equal to the thickness of gate electrode **106**. These post-etch nitride structures are referred to as spacers. As can be seen in Figs. 1-2, that portion of silicon nitride spacer layer **108** that is superjacent to the top surface of gate electrode **106** is removed by the spacer layer etch operation.

Referring to Fig. 3, a plurality of recesses in substrate **102** are produced by using an isotropic dry etch process in a parallel plate RF plasma etching system. A mixture of sulfur

hexafluoride (SF_6) and helium (He), at process conditions that favor isotropy are employed. Such conditions include high pressure and low RF power density. In one embodiment of the present invention, a process pressure of approximately 900 mT, a gap of 1.1 cm, an RF power of 100 W, a He flow of 150 sccm, and a SF_6 flow of 100 sccm is used. RF power may be varied in a range, for example, of 50 W to 200 W, and the process pressure may be varied but should be greater than approximately 500 mT. This etch process is highly selective and is characterized by a silicon etch rate that is much greater than the etch rate of the silicon dioxide that forms gate dielectric layer **104**. Similarly, the etch rate of silicon substrate **102** is much greater than the etch rate of the silicon nitride that forms sidewall spacers **108**. The electrical characteristics of gate dielectric layer **104** are not adversely affected by the etch process that forms the recesses in substrate **102**.

As can be seen in Fig. 3, the recesses include a portion that underlies gate dielectric layer **104**. In the illustrative embodiment, substrate **102** is etched isotropically such that the lateral etch creates a recessed area that reaches underneath not only the spacer but also partially underneath a region defined by overlying gate electrode **106**.

Note that, since silicon nitride spacer layer **108** was removed from the top surface of polysilicon gate electrode **106**, the etch that forms the recess also etches the top surface of polysilicon gate electrode **106**, thereby reducing its height as shown in Fig. 3.

Those skilled in the art and having the benefit of this disclosure will recognize that the operations and structures disclosed above are applicable to the formation of both n-channel FETs (NFETs) and p-channel FETs (PFETs). PFETs and NFETs are structurally similar, however the relative placement of p-type and n-type dopants is different. That is, a PFET includes p-type source/drain terminals in an n-type body, and an NFET includes n-type source/drain terminals in a p-type body.

The illustrative embodiment is described in terms of the formation of a PFET. It should be recognized that the present invention applies to the structure and manufacture of NFETs as well. Referring now to Fig. 4, an epitaxial film of boron doped Si **110** is formed using SiH_2Cl_2

based chemistry such that the deposition is highly selective to nitride spacer **108**, i.e., the film of boron doped Si **110** does not form on, nor adhere to, silicon nitride spacer **108**. However, the recesses are substantially filled by this deposition operation. The recess may be completely filled by this operation. No ex-situ cleaning operations are performed. This is because an external wet clean would tend to damage thin gate dielectric layer **104**. In an alternative embodiment, boron doped SiGe may be used in place of boron doped Si to form the film that fills the recess. Typically, epitaxial film **110** is deposited such that its top surface is above the plane of the original surface of substrate **102**. This can be seen in Fig. 4 by comparing the relative positions of gate dielectric layer **104**, which was formed on the original surface of substrate **102**, with the top surface of Si layer 110. As is further shown in Fig. 4, an epitaxial film of boron doped Si **110** is also formed on top of gate electrode **106**. In this way the thickness of polysilicon gate electrode **106** is increased from its post-etch dimensions.

Still referring to Fig. 4, boron doped Si film **110** is formed by a selective deposition. A selective deposition of silicon, or a silicon alloy such as silicon germanium, forms silicon, or the silicon alloy, on the exposed silicon surfaces. For example, a selective deposition of boron doped silicon creates Si film **110** on the exposed surfaces of silicon substrate **102**, and polysilicon gate electrode **106**. A silicon film can be selectively deposited by heating the wafer to a temperature of approximately 600 °C to 900 °C, providing a deposition gas comprising dichlorosilane (SiH_2Cl_2), and hydrogen (H_2). More particularly, an n-type silicon can be selectively deposited at a temperature of approximately 750°C, with approximately 10 slm H_2, approximately 30 sccm HCl, approximately 100 sccm SiH_2Cl_2, and approximately 180 sccm PH_3, at approximately atmospheric pressure. Such process conditions can deposit a layer approximately 50 nm thick in approximately 6 minutes. A p-type silicon can be selectively deposited at a temperature of approximately 800°C, with approximately 20 slm H_2, approximately 70 sccm HCl, approximately 120 sccm SiH_2Cl_2, and approximately 75 sccm B_2H_6. Such process conditions can deposit a layer approximately 50 nm thick in approximately 155 seconds.

A silicon germanium alloy can be selectively deposited by heating the wafer to a temperature between approximately 700 °C and 750 °C, providing a deposition gas mix comprising dichlorosilane at a rate of between approximately 10 to 100 sccm, 1% hydrogen diluted germane (GeH_4) at a rate of between approximately 10 to 200 sccm, and hydrogen at a rate of approximately 20 slm into a CVD chamber maintained at a pressure between approximately 50 to 760 torr. A dopant gas such as diborane, phosphine, or arsine, can be included in the process gas mix if a doped silicon or silicon alloy film is desired.

A highly doped ($>5x10^{20}$ atoms/cm^3) n-type silicon germanium epitaxial film can be selectively deposited onto silicon surfaces by thermal chemical vapor deposition utilizing a deposition gas mix comprising approximately 10 to 200 sccm GeH_4, approximately 10 to 100 sccm dichlorosilane, 10 to 40 slm H_2, 1 to 200 sccm PH_3, and 15 sccm HCl, while maintaining the substrate at a temperature between 700°C and 750 °C and maintaining a deposition pressure of approximately 165 torr during film deposition. Such a process will form a substantially uniformly doped n-type silicon germanium epitaxial film. Similarly, a p-type silicon germanium alloy can be formed by decomposition of approximately 20 sccm of dichlorosilane, approximately 80 sccm germane, approximately 20 slm H_2 and a p-type dopant source, such as approximately 1 -200 sccm of B_2H_6 at a temperature of approximately 740°C. In order to increase the selectivity of the deposition process, approximately 10 sccm of HCl can be added to the gas mix. Such process conditions can deposit a layer approximately 50 nm thick in approximately 75 seconds.

Those skilled in the art and having the benefit of this disclosure, will recognize that, the deposition operation is such that selectivity to oxide in field oxide regions, or shallow trench isolation regions is also achieved.

Fig. 5 shows the FET structure of Fig. 4 after further processing operations are performed. Conventional processing may be used to form additional sidewall spacers **112** that are disposed along opposing sidewall spacers **108**. Furthermore, conventional processing may be used to form salicided regions **114** over the top surfaces of doped Si regions **110**, that is, the

source/drain extension regions and polysilicon gate electrode **106**. It should be noted that the structure of the present invention is advantageous in the formation of salicided source/drain extensions. For example, when a metal such as nickel, which diffuses in silicon relatively easily, is used to form a nickel salicide layer, lateral diffusion of nickel atoms is stopped by nitride side wall spacers **108** and the nickel atoms therefore do not penetrate into the channel region where they would otherwise adversely affect the electrical characteristics of the MOSFET. It can be seen in Fig. 4, that the thickness of Si **110** and the depth of salicide layer **114** can be varied with the scope of the invention and still benefit from the structure's metal atom diffusion barrier characteristics.

Referring to Fig. 6, in a further alternative embodiment of the present invention, a layer of phosphorous doped Si **111** is epitaxially formed, prior to an in-situ epitaxial formation of boron doped Si **110**. Those skilled in the art and having the benefit of this disclosure will appreciate that other n-type dopants may be used in place of phosphorous. Arsenic is an example of an alternative n-type dopant.

Since the doping concentration of the single crystal epitaxial layer is a function of the gas mixture, temperature, and pressure, in an epitaxial reaction chamber, it is possible to first form a highly doped Si layer (or $Si_{1-x}Ge_x$, x=0 to 0.3) **111** of a first conductivity type (e.g., n-type by doping with phosphorous). Then without exposing the wafer to the atmosphere, changing the gas mixture, temperature, and pressure, such that a highly doped Si layer **110** of a second conductivity type (e.g., p-type by doping with boron) is formed immediately superjacent Si layer **111**. In this way, the recesses in substrate **102** are filled with a bi-layer of single crystal silicon (or $Si_{1-x}Ge_x$, x=0 to 0.3) having a very abrupt junction.

Desirable electrical characteristics may be obtained in this way by having a relatively lightly doped substrate **102** of a first conductivity type, highly doped source/drain terminals **110** of a second conductivity type, and a highly doped region **111** of the first conductivity type disposed between source/drain terminals **110** and lightly doped substrate **102**. Due to the nature of the selective deposition process (described above), highly doped regions **110**, **111**, are not

only highly doped in the source/drain extension regions, but also in the tip-to-gate overlap region. The term tip, is generally used to refer to that portion of the source/drain junction that is subjacent to the gate and adjacent to the channel portion of a FET.

In conjunction with Fig. 7, the operations of fabricating a FET on a wafer in accordance with an illustrative embodiment of the present invention are described. An operation (block **202**) is performed wherein a spacer layer is formed over a patterned gate electrode. In an illustrative embodiment of the present invention, the gate electrode is comprised of polysilicon that has previously been deposited over a gate dielectric layer. The gate dielectric is typically oxidized silicon. In the illustrative embodiment having an oxide gate dielectric and a polysilicon gate electrode, the spacer layer is typically silicon nitride. Those skilled in the art and having the benefit of this disclosure will recognize that the invention is not limited to the combination of an oxide dielectric and polysilicon gate electrode. By way of example and not limitation, the gate dielectric layer may consist of an oxide layer and a nitride layer in combination. Similarly, by way of example and not limitation, the gate electrode may be formed from a metal rather than polysilicon.

After the spacer layer has been formed, it is subjected to an anisotropic etch (block **204**) in which sidewall spacers are formed. During the anisotropic etch, portions of the spacer layer that are superjacent the top surface the gate electrode and the top surface of the wafer are removed. The remaining portion of the spacer layer disposed along the opposing vertical sidewalls of the gate electrode.

Recesses are formed in the wafer (block **206**) at locations where the source/drain terminals of the FET will be located. The recesses are formed by the isotropic etch of the wafer. As is understood in this field, an isotropic etch operation will remove material from the wafer surface both vertically and laterally. The etch chemistry and conditions are preferably chosen such that the etch is highly selective and preferentially etches the wafer rather than the side wall spacers or the gate dielectric layer. In the illustrative embodiment, wherein the wafer is silicon,

the gate dielectric is an oxide of silicon, the gate electrode is polysilicon and the side wall spacers are silicon nitride, a plasma etch with sulfur hexafluoride (SF_6) and helium (He) is used.

After the recesses are formed, the wafer is typically placed in an epitaxial reactor and a first layer of doped crystalline material is formed (block **208**). The crystalline material may be, for example, p-type silicon, p-type silicon germanium, n-type silicon, or n-type silicon germanium. Typically, the conductivity type of the first layer matches the conductivity type of that portion of the wafer where the FET is being fabricated. Those skilled in the art will recognize that various portions of the wafer may be doped and/or counterdoped so as to form wells within which FETs may be formed. For example, n-channel FETs (NFETs) are formed within a p-type region of the wafer, whereas p-channel FETs (PFETs) are formed within an n-type region of the wafer.

After the first layer is formed, a second layer of doped crystalline material is formed (block **210**). The second layer is typically formed without exposing the first layer to the atmosphere. That is, the second layer and first layer are formed in a continuous in-situ operation, in the same reaction chamber simply by changing the gas mixture, temperature, and pressure in the epitaxial reactor. The crystalline material may be, for example, p-type silicon, p-type silicon germanium, n-type silicon, or n-type silicon germanium. Typically, the conductivity type of the second layer is chosen to be opposite that of the first layer. In this way, extremely abrupt junctions can be obtained.

For example, a gate structure of a PFET is formed in a region of a n-type portion of a silicon wafer, and after the source/drain recesses are formed, a first layer of n-doped (e.g., phosphorous) silicon germanium is formed in the recesses, and then a second layer of p-doped (e.g., boron) silicon germanium is formed over the first layer. Both the first and second layers have doping concentrations that are substantially higher than the doping concentration of the n-type portion of the silicon wafer, which forms the body terminal of the PFET. More particularly, the first and second layer are substantially free of counterdopants, whereas the n-type region of

the wafer typically contains both n-type and p-type dopants. A gate structure may be a gate electrode or a gate electrode and adjacent side wall spacers.

A salicidation operation is typically performed to further reduce the sheet resistivity of the source/drain terminals and gate electrode.

Conclusion

Embodiments of the present invention provide a field effect transistor structure having very short channel length and low source/drain extension resistivity, yet operable to produce high drive currents without suffering from the short channel effects that produce significant levels of off-state current. Further embodiments of the present invention provide methods of manufacturing such a structure.

An advantage of particular embodiments of the present invention is that source/drain terminals can be formed without annealing. By eliminating the high temperature step conventionally required to activate the dopants, thermal diffusion is avoided and the very abrupt junctions are maintained.

An advantage of particular embodiments of the present invention is that the raised junctions formed by back filling, in conjunction with the side wall spacers disposed along opposing vertical walls of the gate electrode, substantially prevent lateral diffusion of metal atoms in the transistor channel region during the salicidation operation.

An advantage of particular embodiments of the present invention is placement of active dopants directly in the tip portion of the source/drain terminals.

An advantage of particular embodiments of the present invention is that a very precise doping profile is achieved.

An advantage of particular embodiments of the present invention is that very shallow, highly doped, source/drain terminals can be formed without ion implantation of the tip portion. In some cases, even a deep source/drain implant, typically used to form portions of source/drain terminals that lie further from the channel region, may be eliminated.

It will be understood by those skilled in the art having the benefit of this disclosure that many design choices are possible within the scope of the present invention. For example, structural parameters, including but not limited to, gate insulator thickness, gate insulator materials, gate electrode thickness, sidewall spacer material, inter-layer dielectric material, isolation trench depth, and S/D and well doping concentrations may all be varied from that shown or described in connection with the illustrative embodiments. Similarly, the operation of forming recesses and back filling with doped crystalline material may be repeated to tailor the shape and doping profile of the source/drain terminals.

It will be understood that various other changes in the details, materials, and arrangements of the parts and steps which have been described and illustrated may be made by those skilled in the art having the benefit of this disclosure without departing from the principles and scope of the invention as expressed in the subjoined Claims.

What is claimed is:

1. A microelectronic structure, comprising:

a substrate having a top surface that defines a first plane;

a dielectric disposed superjacent the top surface of the substrate;

a gate electrode disposed superjacent the dielectric, the gate electrode having first side wall spacers disposed along opposing vertical walls thereof;

a source terminal and a drain terminal each disposed, each substantially adjacent one of the first side wall spacers, partially within the substrate and partially above the substrate, the source and drain terminals further having a portion that extends laterally so as to be subjacent at least a portion of the side wall spacers;

wherein the source and drain terminals have top surfaces that define a second plane, the second plane being above the first plane, and the source and drain terminals comprise a doped crystalline semiconductor.

2. The structure of Claim 1, further comprising:

a body, disposed within the substrate, having a first portion and a second portion;

wherein the first portion is of a first conductivity type and a first doping profile, the second portion is of the first conductivity type and a second doping profile, and a transition between the first doping profile and the second doping profile is abrupt.

3. The structure of Claim 2, wherein the first portion includes counterdopants and the second portion is substantially free of counterdopants.

4. The structure of Claim 1, wherein the gate electrode comprises polysilicon disposed over the gate dielectric; and crystalline silicon of a first conductivity type disposed over the polysilicon.

5. The structure of Claim 4, wherein the gate electrode further comprises a crystalline silicon of a second conductivity type.

6. The structure of Claim 1, further comprising second side wall spacers adjacent the first side wall spacers; and metal salicide disposed in an upper portion of the gate electrode and an upper portion of the source/drain terminals.

7. The structure of Claim 6, wherein the source/drain terminals comprise p-type silicon.

8. The structure of Claim 6, wherein the source/drain terminals comprise n-type silicon.

9. The structure of Claim 6, wherein the source/drain terminals comprise p-type silicon germanium.

10. The structure of Claim 6, wherein the source/drain terminals comprise n-type silicon germanium.

11. A method of making a junction, comprising:

a) forming a patterned structure on a surface of a substrate, the substrate being of a first conductivity type;

b) isotropically etching the substrate such that a recess in the substrate is formed, the recess including a portion that underlies the patterned structure, the recess having a surface; and

c) selectively forming a layer of a first material having a second conductivity type in the recess.

12. The method of Claim 11, further comprising, prior to selectively forming the layer of the first material, selectively forming a layer of a second material having the first conductivity type over the surface of the recess.

13. The method of Claim 12, wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon, and the second material comprises doped silicon.

14. The method of Claim 12, wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon germanium, and the second material comprises doped silicon germanium.

15. The method of Claim 14, wherein the second material has a thickness that is less than a thickness of the first material.

16. The method of Claim 15, wherein the first material has a top surface that is above a plane defined by the surface of the substrate.

17. The method of Claim 11, wherein the patterned structure comprises a dielectric layer and a conductive material disposed over the dielectric layer.

18. The method of Claim 11, wherein etching passivates the surface of the recess.

19. The method of Claim 11, wherein etching comprises exposing the substrate to SF_6 and He in an RF plasma etching system.

20. The method of Claim 11, wherein forming the first material comprises epitaxially depositing a layer of crystalline material.

21. The method of Claim 11, wherein forming the first material comprises epitaxially depositing a layer of crystalline material; and forming the second material comprises epitaxially depositing a layer of crystalline material; wherein the substrate remains unexposed to the atmosphere subsequent to forming the first material and prior to forming the second material.

22. A method of making a transistor, comprising:

forming a dielectric on a first surface of a wafer;

forming a conductive layer overlying the dielectric;

patterning the conductive layer and dielectric so as to form a gate structure;

forming recesses adjacent and partially subjacent the gate structure; and

in a continuous operation, back filling the recesses with doped crystalline material;

wherein back filling comprises forming crystalline material of at least a first conductivity type.

23. The method of Claim 22, wherein the crystalline material of the first conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium.

24. The method of Claim 22, wherein back filling further comprises forming crystalline material of a second conductivity type.

25. The method of Claim 22, wherein the crystalline material of the second conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium.

26. The method of Claim 25, wherein back filling comprises a selective deposition.

27. A method of fabricating a FET, comprising:

forming a gate electrode having side walls over a gate insulator on a surface of a semiconductor substrate having a first conductivity type;

forming first spacers along the sidewalls of the gate electrode;

forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface;

substantially filling the recess with a fist layer of doped crystalline material, the first layer having a second conductivity type.

28. The method of Claim 27, further comprising depositing the first layer of doped crystalline material until a vertical distance between a top surface of the first layer and the surface of the substrate is greater than a vertical distance between a top surface of the gate insulator and the surface of the substrate.

29. The method of Claim 27, further comprising forming a second layer of doped crystalline material over the substrate surface of the recess, the second layer having the same conductivity type as the semiconductor substrate, and the second layer having a doping concentration that is greater than a doping concentration of the semiconductor substrate near the substrate surface of the recess.

30. The method of Claim 29, wherein forming a recess comprises placing the substrate in a parallel plate reaction chamber with a gap of approximately 1.1 cm, an RF power in the range of

approximately 50 W to 200 W, a pressure greater than approximately 500 mT, and plasma etching with sulfur hexafluoride and helium.

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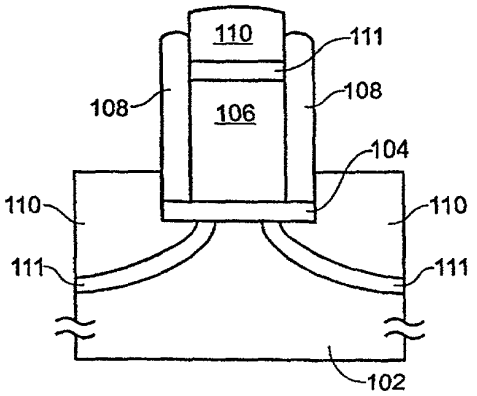

(57) Abstract

Microelectronic structures embodying the present invention include a field effect transistor (FET) having highly conductive source/drain extensions. Formation of such highly conductive source/drain extensions includes forming a passivated recess which is back filled by epitaxial deposition of doped material to form the source/drain junctions. The recesses include a laterally extending region that underlies a portion of the gate structure. Such a lateral extension may underlie a sidewall spacer (108) adjacent to the vertical sidewalls of the gate electrode (106), or may extend further into the channel portion of a FET such that the lateral recess underlies the gate electrode portion of the gate structure. In one embodiment the recess is back filled by an in-situ epitaxial deposition of a bilayer of oppositely doped material. In this way, a very abrupt junction is achieved that provides a relatively low resistance source/drain extension and further provides good off-state subthreshold leakage characteristics. Alternative embodiments can be implemented with a back filled recess of a single conductivity type.

Fig. 1

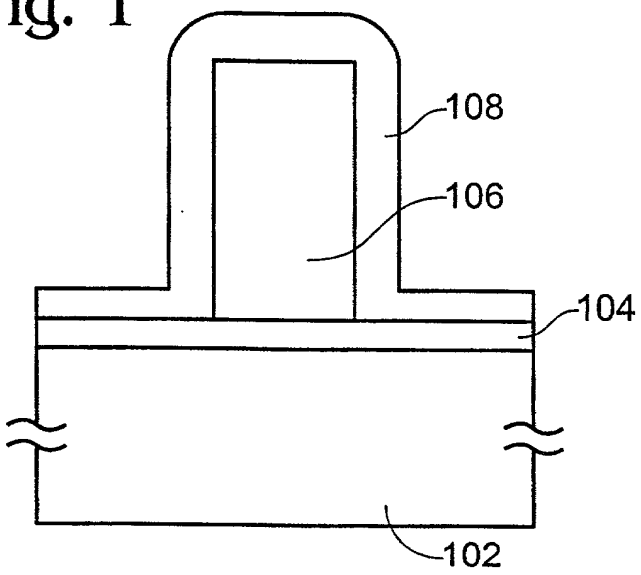

Fig. 2

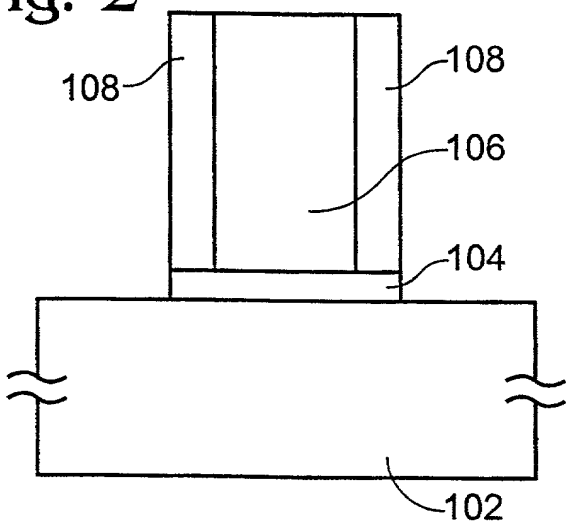

Fig. 3

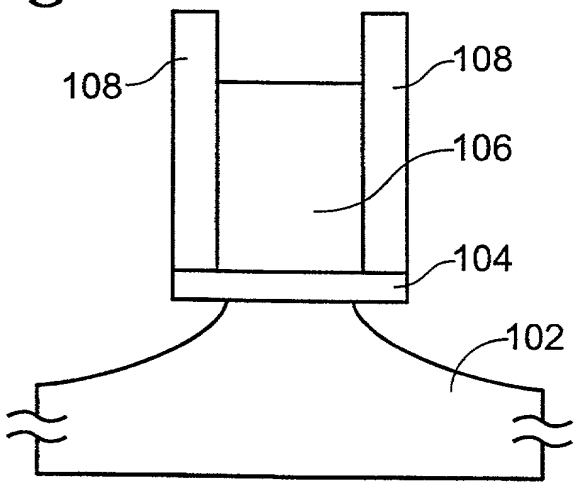

Fig. 4

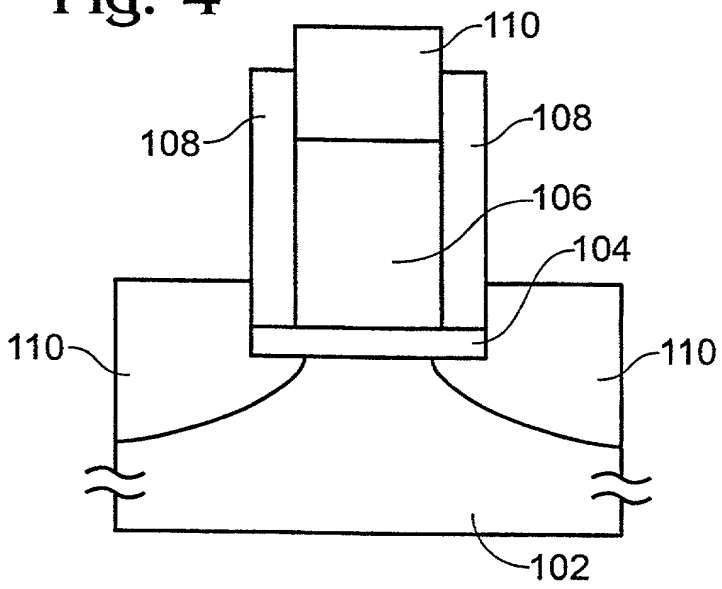

Fig. 5

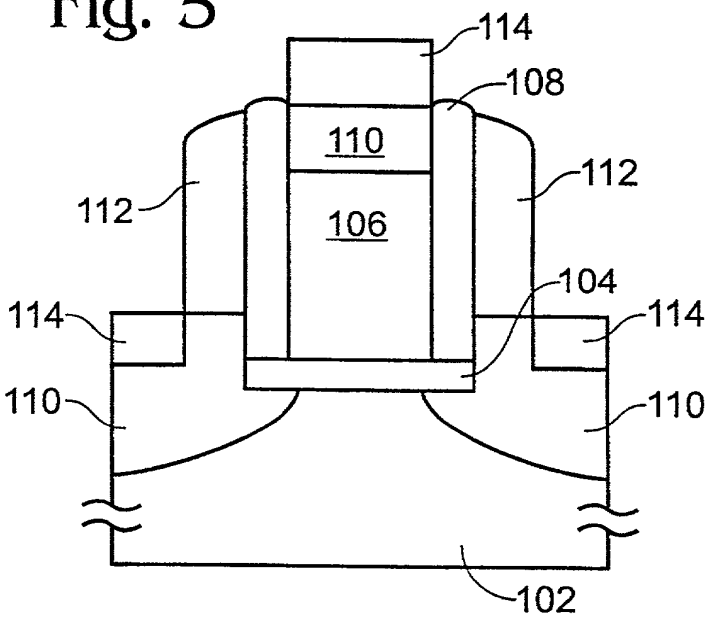
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Fig. 6

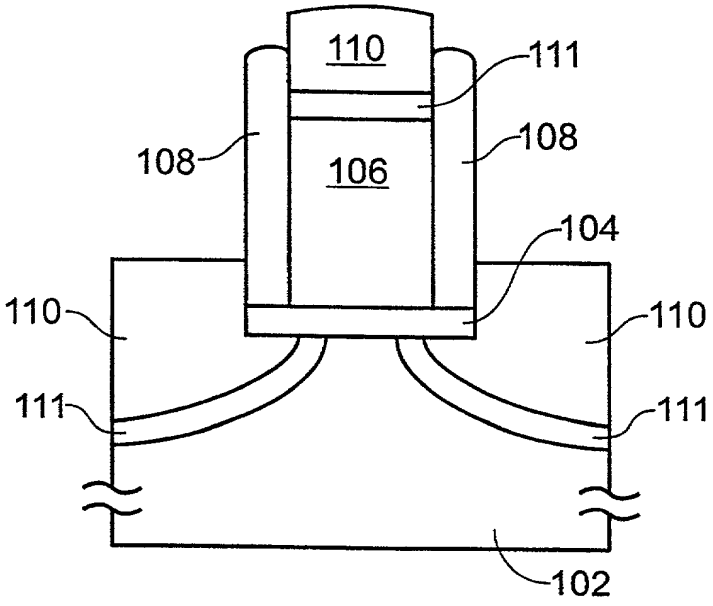
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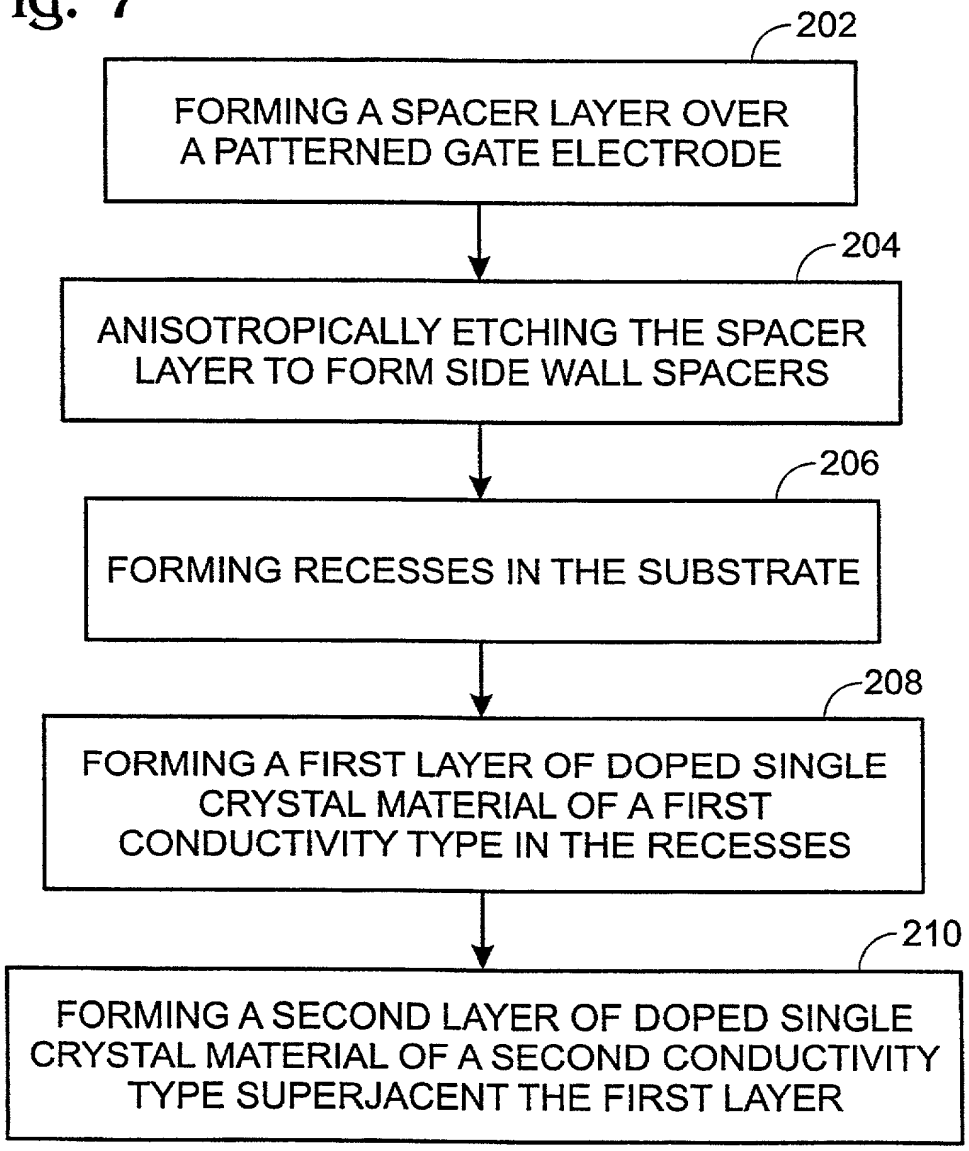
Fig. 7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210
FORMING A SECOND LAYER OF DOPED SINGLE CRYSTAL MATERIAL OF A SECOND CONDUCTIVITY TYPE SUPERJACENT THE FIRST LAYER

Attorney's Docket No.: 42390P6624US

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

FIELD EFFECT TRANSISTOR STRUCTURE WITH ABRUPT SOURCE/DRAIN JUNCTIONS

the specification of which
☐ is attached hereto.
☒ was filed on 11/05/1999 ✓ as
United States Application Number 09/831,539 ✓
or PCT International Application Number PCT/US99/26224 ✓
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application. I do not know and do not believe that the claimed invention was in public use or on sale in the United States of America more than one year prior to this application, nor do I know or believe that the invention has been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
PCT/US99/26224 ✓	PCT ✓	11/12/1998 ✓	☐ No ☒ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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